Ordering number : ENN*6749

CMOS IC

LC86E7248

8-Bit Single Chip Microcontroller with the UVEPROM

Preliminary

Overview

The LC86E7248 is a CMOS 8-bit single chip microcontroller with UVEPROM for the LC867200 series. This microcontroller has the function and the pin description of the LC867200 series mask ROM version, and 48K-byte EPROM. The program data is rewritable. It is suitable to develop the program.

Features

(1) Option switching by EPROM data
The option function of the LC867200 series can be specified by the EPROM data.
LC86E7248 can be checked the functions of the trial pieces using the mass production board.
(2) Internal EPROM capacity : 49408 bytes
(3) Internal RAM capacity : 1152 bytes
Used EPROM or RAM capacity are equal ROM or RAM capacity of mask ROM version which applies LC86E7248.

Mask ROM version	EPROM capacity	RAM capacity
LC867248	49152 bytes	1152 bytes
LC867240	40960 bytes	1152 bytes
LC867232	32768 bytes	1152 bytes
LC867224	24576 bytes	1152 bytes

(4) Operating supply voltage : 4.5V to 6.0V
(5) Instruction cycle time : 1µs to 366µs
(6) Operating temperature : +10°C to +40°C
(7) The pin compatible with the LC867200 series mask ROM devices
(8) Applicable mask ROM version : LC867248/40/32/24
(9) Factory shipment : QFC100S (with window)

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Notice for use

At using, take notice of the followings.

(1) A point of difference LC86E7248 and LC867200 series

Item	LC86E7248	LC867248/40/32/24
Operation after reset releasing	The option is specified until 3ms after going to a 'H' level to the reset terminal by degrees. The program is executed from 00H of the program counter.	The program is executed from 00H of the program counter immediately after going to a 'H' level to the reset terminal.
Operating supply voltage range (VDD)	4.5V to 6.0V	2.5V to 6.0V
Operating temperature range (Topr)	+10°C to +40°C	-30°C to +70°C
Power dessipation	Refer to 'electrical characteristics' on the semiconductor news.	

LC86E7248 uses 256 bytes that is addressed on 0FF00H to FFFFH in the program memory as the option configuration data area. This option configuration cannot execute all options which LC867200 series have. Next tables show the options that correspond and not correspond to LC86E7248.

• A kind of the option corresponding of the LC86E7248

A kind of option	Pins, Circuits	Contents of the option
Input/output form of input/output ports	Port 0	1. N-channel open drain output 2. CMOS output *1
		1. Pull-up MOS Tr. 2. No Pull-up MOS Tr. *2
	Port 1 *1	1. Input : Programmable pull-up MOS Tr. Output : N-channel open drain 2. Input : Programmable pull-up MOS Tr. Output : CMOS
	Port 3 *1	1. Input : No Programmable pull-up MOS Tr. Output : N-channel open drain 2. Input : Programmable pull-up MOS Tr. Output : CMOS
Pull-up MOS Tr. of input port	Ports 70, 71, 72, 73 *1	1. No Pull-up MOS Tr. 2. Pull-up MOS Tr.

*1) Specified in a bit.
*2) Specified in nibble unit. Pull-up MOS Tr. is not provided in N-channel open drain output port.

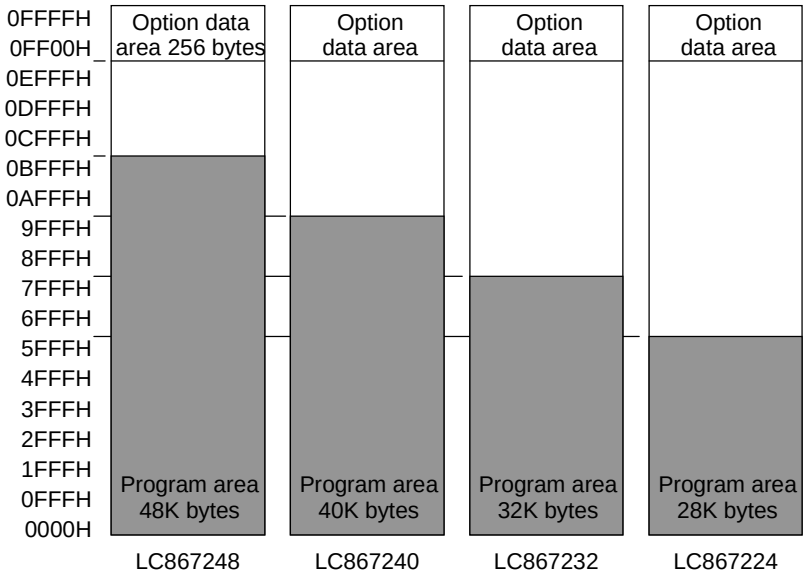
The port operation related the option is different at reset. Refer to the next table.

(1) Option

The option data is created by the option specified program “SU86K.EXE”. The created option data is linked to the program area by linkage loader “L86K.EXE”.

(2) ROM space

LC86E7248 and LC867200 series use 256 bytes that is addressed on 0FF00H to 0FFFFH in the program memory as the option specified data area. These program memory capacity are 49152 bytes that is addressed on 0000H to 0BFFFH.



How to use

(1) Specification of option

Programming data for PROM of the LC86E7248 is required.

Debugged evaluation file (EVA file) must be converted to an INTEL-HEX formatted file (HEX file) with file converter program, EVA2HEX.EXE. The HEX file is used as the programming data for the LC86P6548.

(2) How to program for the EPROM

The LC86E7248 can be programmed by EPROM programmer with attachment ; W86EP7248Q

• Recommended EPROM programmer

Productor	EPROM programmer
Advantest	R4945, R4944, R4943
Andou	AF-9704
AVAL	PKW-1100, PKW-3000
Minato electronics	MODEL1890A

• "27512 (Vpp=12.5V) Intel high speed programming" mode available. The address must be set to "0 to 0FFFFH" and a jumper (DASEC) must be set to 'OFF' at programming.

(3) How to use the data security function

"Data security" is the disabled function to read the data of the EPROM.

The following is the process in order to execute the data security.

1. Set 'ON' the jumper of attachment.
2. Program again. Then EPROM programmer displays the error. The error means normally activity of the data security. It is not a trouble of the EPROM programmer or the LSI.

Notes

• Data security is not executed when the data of all address have 'FFH' at the sequence 2 above.

• The programming by a sequential operation "BLANK=>PROGRAM=>VERIFY" cannot be executed data security at the sequence 2 above.

• Set to 'OFF' the jumper after executing the data security.

(4) How to eliminate

The programming data can be erased by using the EPROM eraser.

(5) Shielding

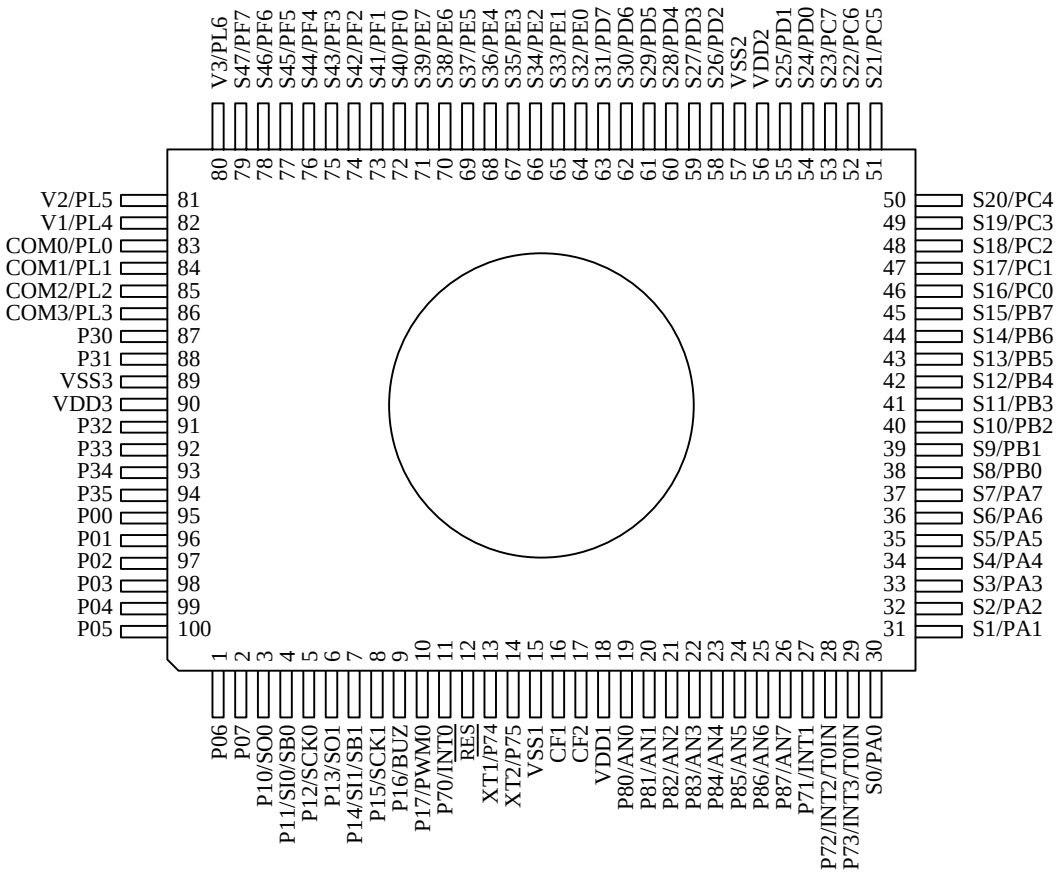
The UVEPROM (ultraviolet erasable programmable ROM) is in it. Put the seal on the window in use.

Data security

Not data security

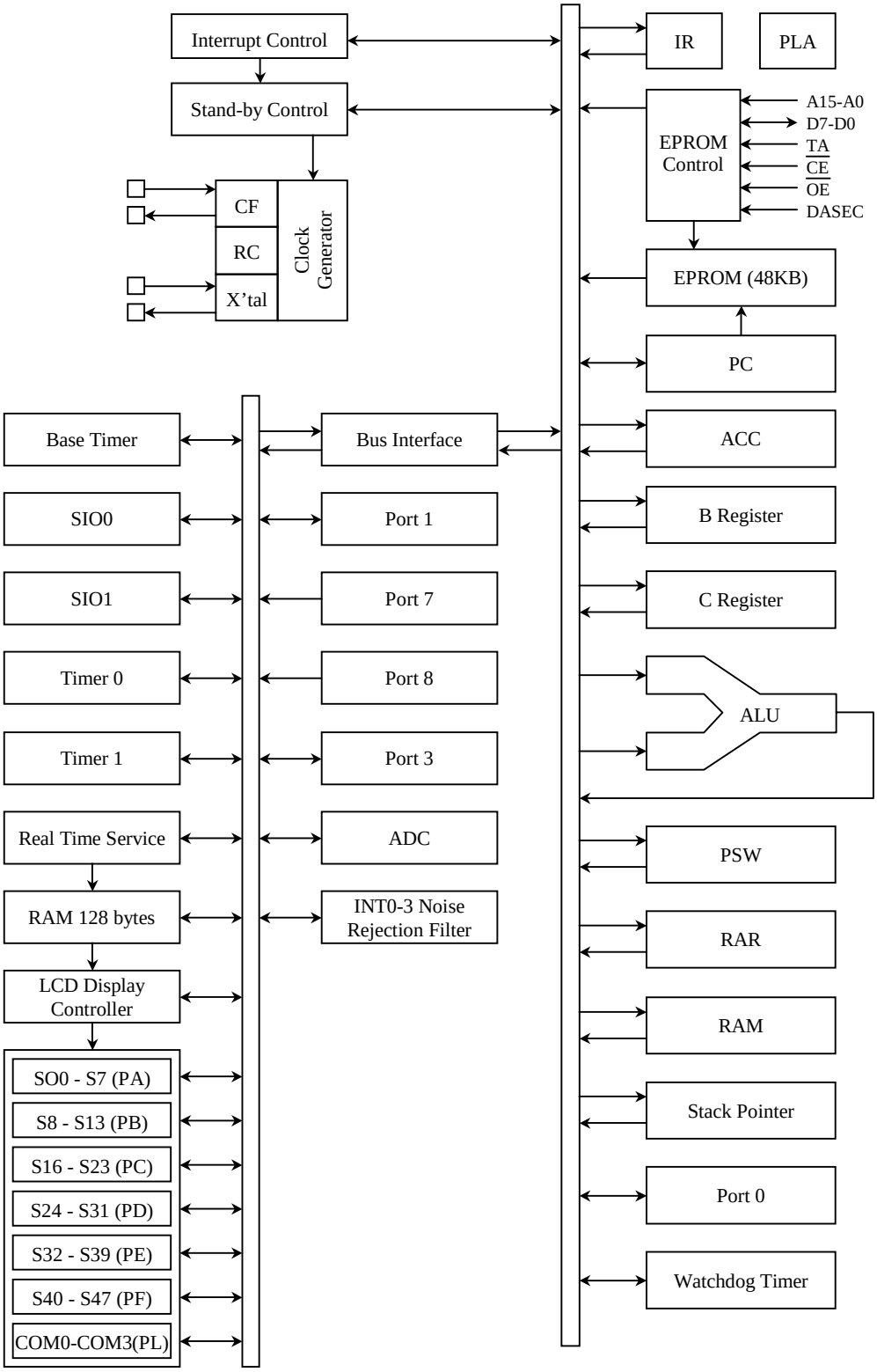
W86EP7248Q

Pin Assignment



SANYO : QFC100S

System Block Diagram



Pin Description

<table>
<tr><th>Pin name</th><th>I/O</th><th>Function description</th><th>Option</th><th>PROM mode</th></tr>
<tr><td>VSS1, 2, 3
*1</td><td>-</td><td>Power pin (–)</td><td>-</td><td>-</td></tr>
<tr><td>VDD1, 2, 3
*1</td><td>-</td><td>Power pin (+)</td><td>-</td><td>-</td></tr>
<tr><td>PORT0
P00 - P07</td><td>I/O</td><td>• 8-bit input/output port
Input/output in nibble units
• Input for port 0 interrupt
• Input for HOLD release</td><td>• Pull-up resistor :
Provided/Not provided
(specified in nibble units)
• Output form (P00 – P07) :
CMOS/N-channel open drain
(specified in a bit)</td><td>-</td></tr>
<tr><td>PORT1
P10 - P17</td><td>I/O</td><td>• 8-bit input/output port
Input/output can be specified in bit unit
• Other pin functions
P10 : SIO0 data output
P11 : SIO0 data input/bus input/output
P12 : SIO0 clock input/output
P13 : SIO1 data output
P14 : SIO1 data input/bus input/output
P15 : SIO1 clock input/output
P16 : Buzzer output
P17 : Timer1 output (PWM output)</td><td>• Output form :
CMOS/N-channel open drain
(specified in a bit)</td><td>Data line
D0 to D7</td></tr>
<tr><td>PORT3
P30 - P35</td><td>I/O</td><td>• 6-bit input/output port
• Input/output can be specified in bit unit</td><td>• Output form :
CMOS/N-channel open drain
(specified in a bit)</td><td>-</td></tr>
<tr><td>PORT7

P70

P71 - P73

$\overline{\text{P74}}$, P75</td><td>

I/O

I

I</td><td>• 6-bit input port
• Other pin functions
P70 : INT0 input/HOLD release input/
N-ch Tr. output for watchdog timer
P71 : INT1 input/HOLD release input
P72 : INT2 input/timer 0 event input
P73 : INT3 input with noise filter/timer 0
event input
• Interrupt received form, vector address
<table>
<tr><th></th><th>rising</th><th>falling</th><th>rising & falling</th><th>high level</th><th>low level</th><th>vector</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>03H</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>0BH</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>13H</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>1BH</td></tr>
</table>
$\overline{\text{P74}}$: XT1 terminal for crystal oscillation
P75 : XT2 terminal for crystal oscillation</td><td>Pull-up resistor :
Provided/Not provided
(specified in a bit)
(P70, P71, P72, P73)
* $\overline{\text{P74}}$, P75 don’t have the pull-up resistor option.</td><td>
Power for programming

PROM control signals
DASEC (*2)
$\overline{\text{OE}}$ (*3)
$\overline{\text{CE}}$ (*4)</td></tr>
<tr><td>Port8
P80 – P87</td><td>I</td><td>• 8-bit input port
• Other function
AD input port (8 port pins)</td><td>-</td><td>-</td></tr>
</table>

Pin name	I/O	Function description	Option	PROM mode
Port A (S0/PA0 – S7/PA7)	I/O	• Segment output terminal for LCD display • Can be used as a general input/output port	-	Address input A0 to A7
Port B (S8/PB0 – S15/PB7)	I/O	• Segment output terminal for LCD display • Can be used as a general input/output port	-	Address input A8 to A13
Port C (S16/PC0 – S23/PC7)	I/O	• Segment output terminal for LCD display • Can be used as a general input/output port	-	PROM control signal input • TA (*5) Address input • A14, A15
Port D (S24/PD0 – S31/PD7)	I/O	• Segment output terminal for LCD display • Can be used as a general input/output port	-	-
Port E (S32/PE0 – S39/PE7)	I/O	• Segment output terminal for LCD display • Can be used as a general input/output port	-	-
Port F (S40/PF0 – S47/PF7)	I/O	• Segment output terminal for LCD display • Can be used as a general input/output port	-	-
Port L (COM0/PL0 – COM3/PL3)	I/O	• Common output terminal for LCD display • Can be used as a general input port	-	-
V1/PL4 – V3/PL6	I	• Bias power terminal for LCD drive • Can be used as a general input port	-	-
$\overline{\text{RES}}$	I	Reset pin	-	-
XT1/ $\overline{\text{P74}}$	I	• Input pin for 32.768kHz crystal oscillation In case of non use, connect to VDD. • Other function A general input port $\overline{\text{P74}}$	-	-
XT2/P75	O (I)	• Output pin for 32.768kHz crystal oscillation In case of non use, should be left unconnected • Other function A general input port P75	-	-
CF1	I	Input pin for ceramic resonator oscillation	-	-
CF2	O	Output pin for ceramic resonator oscillation	-	-

* All of port options can be specified in a bit unit except the pull-up resistor of port 0.

[Notes] • The VDD1, VDD2 and VDD3 terminals must be shorted electrically each other.
• The VSS1, VSS2 and VSS3 terminals must be shorted electrically each other.

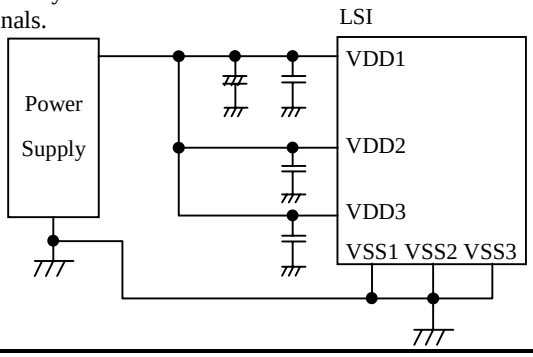
*1 Connect like the following figure to reduce noise into a VDD terminals.

*2 Memory select input for data security

*3 Output enable input

*4 Chip enable input

*5 TA → PROM control signal input



1. Absolute Maximum Ratings at Ta=25°C, VSS=VSS1=VSS2=VSS3=0V

Parameter		Symbol	Pins	Conditions	Ratings				unit
					VDD[V]	min.	typ.	max.	
Supply voltage		VDDMAX	VDD1, VDD2 VDD3	VDD1=VDD2= VDD3		-0.3		+7.0	V
LCD display voltage		VLCD	V1/PL6, V2/PL5 V3/PL4	VDD1=VDD2= VDD3		-0.3		VDD	
Input voltage		VI	•Ports 71, 72, 73 •Ports $\overline{74}$, 75 •Port 8, Port L • $\overline{\text{RES}}$			-0.3		VDD+0.3	
Input/output voltage		VIO	•Port 0, 1, 3 •Port 70 •Ports A,B,C,D,E,F			-0.3		VDD+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 3	•CMOS output •At each pins		-4			mA
		IOPH(2)	Ports A,B,C,D,E,F			-4			
	Total output current	ΣIOAH(1)	Ports 0, 1, 32, 33, 34, 35	Total all pins		-38			
		ΣIOAH(2)	Ports 30, 31	Total all pins		-4			
		ΣIOAH(3)	Ports S0 to S25	Total all pins		-25			
		ΣIOAH(4)	Ports S26 to S47	Total all pins		-25			
Low level output current	Peak output current	IOPL(1)	Ports 0, 1, 3	At each pins				20	
		IOPL(2)	Ports A,B,C,D,E,F	At each pins				20	
		IOPL(3)	Port 70	At each pins				15	
	Total output current	ΣIOAL(1)	Ports 0, 1, 32, 33, 34, 35	Total all pins				50	
		ΣIOAL(2)	Ports 30, 31	Total all pins				20	
		ΣIOAL(3)	Ports S0 to S25	Total all pins				39	
		ΣIOAL(4)	Ports S26 to S47	Total all pins				33	
		ΣIOAL(5)	Port 70	Total all pins				10	
Maximum power dissipation		Pdmax	QFC100S	Ta=+10 to+40°C				515	mW
Operating temperature range		Topr				+10		+40	°C
Storage temperature range		Tstg				-55		+125	

2. Recommended Operating Range at Ta=+10°C to +40°C, VSS =0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Operating supply voltage range	VDD(1)	VDD1, VDD2, VDD3	0.98μs ≤ tCYC ≤ 400μs		4.5		6.0	V
	VDD(2)		3.9μs ≤ tCYC ≤ 400μs		2.5		6.0	
Hold voltage	VHD	VDD1, VDD2, VDD3	RAMs and the registers hold voltage at HOLD mode.		2.0		6.0	
Input high voltage	VIH(1)	Port 0	Output disable	4.5-6.0	0.4VDD +0.9		VDD	
	VIH(2)	•Ports 1, 3 •Ports A,B,C,D,E,F,L •Ports 72, 73	Output disable	4.5-6.0	0.75VDD		VDD	
	VIH(3)	•Port 70 Port input/interrupt •Port 71 • $\overline{\text{RES}}$	Output N-channel Tr. OFF	4.5-6.0	0.75VDD		VDD	
	VIH(4)	Port 70 Watchdog timer	Output N-channel Tr. OFF	4.5-6.0	0.9VDD		VDD	
	VIH(5)	•Port 8	Output N-channel Tr. OFF	4.5-6.0	0.75VDD		VDD	
Input low voltage	VIL(1)	Port 0	Output disable	4.5-6.0	VSS		0.2VDD	
	VIL(2)	•Ports 1, 3 •Ports A,B,C,D,E,F,L •Ports 72, 73	Output disable	4.5-6.0	VSS		0.25VDD	
	VIL(3)	•Port 70 Port input/interrupt •Port 71 • $\overline{\text{RES}}$	Output N-channel Tr. OFF	4.5-6.0	VSS		0.25VDD	
	VIL(4)	Port 70 Watchdog timer	Output N-channel Tr. OFF	4.5-6.0	VSS		0.8VDD -1.0	
	VIL(5)	•Port 8	Output N-channel Tr. OFF	4.5-6.0	VSS		0.25VDD	
Operation cycle time	tCYC			4.5-6.0	0.98		400	μs
				4.5-6.0	3.9		400	
Oscillation frequency range (Note 1)	FmCF(1)	CF1, CF2	•6MHz (ceramic resonator oscillation) •Refer to figure 1	4.5-6.0		6		MHz
	FmCF(2)	CF1, CF2	•3MHz (ceramic resonator oscillation) •Refer to figure 1	4.5-6.0		3		
	FmRC		RC oscillation	4.5-6.0	0.4	0.8	3.0	
	FsXtal	XT1, XT2	•32.768kHz (crystal oscillation) •Refer to figure 2	4.5-6.0		32.768		kHz
Oscillation stabilizing time period (Note 1)	tmsCF(1)	CF1, CF2	•6MHz (ceramic resonator oscillation) •Refer to figure 3	4.5-6.0				ms
	tmsCF(2)	CF1, CF2	•3MHz (ceramic resonator oscillation) •Refer to figure 3	4.5-6.0				
	tssXtal	XT1, XT2	•32.768kHz (crystal oscillation) •Refer to figure 3	4.5-6.0				s

(Note 1) The oscillation constant is shown on table 1 and table 2.

3. Electrical Characteristics at Ta=+10°C to +40°C, VSS=VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Input high current	IIH(1)	•Port 1 •Port 0 without pull-up MOS Tr.	•Output disable •Pull-up MOS Tr. OFF. VIN=VDD (including the off-leak current of the output Tr.)	4.5-6.0			1	μA
	IIH(2)	•Port 7 without pull-up MOS Tr. •Port 8	VIN=VDD	4.5-6.0			1	
	IIH(3)	Port 3	VIN=VDD	4.5-6.0			1	
	IIH(4)	Ports A,B,C,D,E,F,L	VIN=VDD	4.5-6.0			1	
	IIH(5)	$\overline{RES}$	VIN=VDD	4.5-6.0			1	
	IIH(6)	Ports $\overline{74}$,75	Using as port VIN=VDD	4.5-6.0			1	
Input low current	IIL(1)	•Port 1 •Port 0 without pull-up MOS Tr.	•Output disable •Pull-up MOS Tr. OFF. VIN=VSS (including the off-leak current of the output Tr.)	4.5-6.0	-1			
	IIL(2)	•Port 7 without pull-up MOS Tr. •Port 8	VIN=VSS	4.5-6.0	-1			
	IIL(3)	Port 3	VIN=VSS	4.5-6.0	-1			
	IIL(4)	Ports A,B,C,D,E,F,L	VIN=VSS	4.5-6.0	-1			
	IIL(5)	$\overline{RES}$	VIN=VSS	4.5-6.0	-1			
	IIL(6)	Ports $\overline{74}$,75	Using as port VIN=VSS	4.5-6.0	-1			
Output high voltage	VOH(1)	Ports 0,1 of CMOS output	IOH=-1.0mA	4.5-6.0	VDD-1			V
	VOH(2)	•Port 3 of CMOS output •Ports A,B,C,D,E,F of CMOS output	IOH=-1.0mA	4.5-6.0	VDD-1			
Output low voltage	VOL(1)	Ports 0, 1	IOL=10mA	4.5-6.0			1.5	
	VOL(2)		IOL=1.6mA	4.5-6.0			0.4	
	VOL(3)	Port 70	IOL=1mA	4.5-6.0			0.4	
	VOL(4)	Port 3	IOL=10mA	4.5-6.0			1.5	
	VOL(5)		IOL=1.6mA	4.5-6.0			0.4	
	VOL(6)	Ports A,B,C,D,E,F of CMOS output	IOL=8mA	4.5-6.0			1.5	
	VOL(7)		IOL=1.6mA	4.5-6.0			0.4	

Continue.

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
LCD output regulation	VODLS	S0 to S47	•Deference voltage to ideal value •VLCD, 2/3VLCD, 1/3VLCD	4.5-6.0	0		±0.2	V
	VODLC	COM0 to COM3	•Deference voltage to ideal value •VLCD, 2/3VLCD, 1/2VLCD, 1/3VLCD	4.5-6.0	0		±0.2	
LCD ladder resistor	RLCD(1)		Resistance at a ladder resistor	4.5-6.0		60		kΩ
	RLCD(2)		•Resistance at a ladder resistor •1/2R mode	4.5-6.0		30		
Pull-up MOS Tr. resistor	Rpu	•Ports 0, 1, 3 •Ports A,B,C,D,E,F •Ports 70, 71, 72, 73	VOH=0.9VDD	4.5-6.0	15	40	70	
Hysteresis voltage	VHIS	•Port 1 •Ports 70, 71, 72, 73 • $\overline{\text{RES}}$	Output disable	4.5-6.0		0.1VDD		V
Pin capacitance	CP	All pins	•f=1MHz •Unmeasurement terminals for the input are set to VSS level. •Ta=25°C	4.5-6.0		10		pF

4. Serial Input / Output Characteristics at Ta=+10°C to +40°C, VSS=VSS1=VSS2=VSS3=0V

Parameter			Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Serial clock	Input clock	Cycle	tCKCY(1)	SCK0, SCK1	Refer to figure 5.	4.5-6.0	2			tCYC
		Low Level pulse width	tCKL(1)				1			
		High Level pulse width	tCKH(1)				1			
	Output clock	Cycle	tCKCY(2)	SCK0, SCK1	•Use pull-up resistor (1kΩ) when open drain output. •Refer to figure 5.	4.5-6.0	2			
		Low Level pulse width	tCKL(2)					1/2 tCKCY		
		High Level pulse width	tCKH(2)					1/2 tCKCY		
Serial input	Data set up time		tICK	•SI0,SI1 •SB0,SB1	•Data set-up to SCK0, 1 •Data hold from SCK0, 1 •Refer to figure 5.	4.5-6.0	0.1			µs
	Data hold time		tCKI			4.5-6.0	0.1			
Serial output	Output delay time (Serial clock is external clock)		tCKO(1)	•SO0, SO1 •SB0, SB1	•Use pull-up resistor (1kΩ) when open drain output. •Data hold from SCK0, 1 •Refer to figure 5.	4.5-6.0			7/12tCYC +0.2	
	Output delay time (Serial clock is internal clock)		tCKO(2)			4.5-6.0			1/3tCYC +0.2	

5. Pulse Input Conditions at Ta=+10°C to +40°C, VSS=VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions	Ratings			unit
				VDD[V]	min.	typ.	max.	
High/low level pulse width	tPIH(1) tPIL(1)	•INT0, INT1 •INT2/T0IN	•Interrupt acceptable •Timer0-countable	4.5-6.0	1			tCYC
	tPIH(2) tPIL(2)	INT3/T0IN (The noise rejection clock is selected to 1/1.)	•Interrupt acceptable •Timer0-countable	4.5-6.0	2			
	tPIH(3) tPIL(3)	INT3/T0IN (The noise rejection clock is selected to 1/16.)	•Interrupt acceptable •Timer0-countable	4.5-6.0	32			
	tPIH(4) tPIL(4)	INT3/T0IN (The noise rejection clock is selected to 1/64.)	•Interrupt acceptable •Timer0-countable	4.5-6.0	128			
	tPIL(5)	$\overline{\text{RES}}$	Reset acceptable	4.5-6.0	200			µs

6. AD Converter Characteristics at Ta=+10°C to + 40°C, VSS=VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions	Ratings			unit
				VDD[V]	min.	typ.	max.	
Resolution	NAD			4.5-6.0		8		bit
Absolute precision (Note 2)	ETAD			4.5-6.0			±1.5	LSB
Conversion time	tCAD		AD conversion time = 16 × tCYC (ADCR2=0) (Note 3)	4.5-6.0	15.68 (tCYC= 0.98µs)		65.28 (tCYC= 4.08µs)	µs
			AD conversion time = 32 × tCYC (ADCR2=1) (Note 3)		31.36 (tCYC= 0.98µs)		130.56 (tCYC= 4.08µs)	
Analog input voltage range	VAIN	AN0 - AN7		4.5-6.0	VSS		VDD	V
Analog port input current	IAINH		VAIN=VDD	4.5-6.0			1	µA
	IAINL		VAIN=VSS	4.5-6.0	-1			

(Note 2) Absolute precision excepts quantizing error (±1/2 LSB).

(Note 3) The conversion time means the time from executing the AD conversion instruction to setting the complete digital conversion value to the register.

7. Current Dissipation Characteristics at Ta=+10°C to +40°C, VSS=VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions	Ratings				unit
				VDD[V]	min.	typ.	max.	
Current dissipation during basic operation (Note 4)	IDDOP(1)	VDD1= VDD2= VDD3	•FmCF=6MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops •1/1 divided	4.5-6.0		15	30	mA
	IDDOP(2)		•FmCF=3MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops •1/2 divided	4.5-6.0		6	15	
	IDDOP(3)		•FmCF=0Hz (when oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : RC oscillation •1/2 divided	4.5-6.0		4	13	
	IDDOP(4)		•FmCF=0Hz (when oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : crystal oscillation •Internal RC oscillation stops •1/2 divided	4.5-6.0		4	9	

Continue.

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Current dissipation in HALT mode (Note 4)	IDDHALT(1)	VDD1= VDD2= VDD3	•HALT mode •FmCF=6MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops •1/1 divided	4.5-6.0		6	11	mA
	IDDHALT(2)		•HALT mode •FmCF=3MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops •1/2 divided	4.5-6.0		2.2	9	
	IDDHALT(3)		•HALT mode FmCF=0Hz (when oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : RC oscillation •1/2 divided	4.5-6.0		500	1700	μA
	IDDHALT(4)		•HALT mode FmCF=0Hz (when oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : crystal oscillation •Internal RC oscillation stops •1/2 divided	4.5-6.0		25	100	
	IDDHALT(5)							
Current dissipation in HOLD mode (Note 4)	IDDHOLD(1)	VDD1= VDD2= VDD3	HOLD mode	4.5-6.0		0.05	30	

(Note 4) The currents of the output transistors and the pull-up MOS transistors are ignored.

Table 1. Ceramic resonator oscillation guaranteed constant (main clock)

Oscillation type	Maker	Oscillator	C1	C2
6MHz ceramic resonator oscillation				
3MHz ceramic resonator oscillation				

* Both C1 and C2 must use K rank (±10%) and SL characteristics.

Table 2. Crystal oscillation recommended constant (sub clock)

Oscillation type	Maker	Oscillator	C3	C4	Rd
32.768kHz crystal oscillation					

* Both C3 and C4 must use J rank (±5%) and CH characteristics.
(It is about the application which is not in need of high precision. Use K rank (±10%) and SL characteristics.)

(Notes) •Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.
•If you use other oscillators herein, we provide no guarantee for the characteristics.

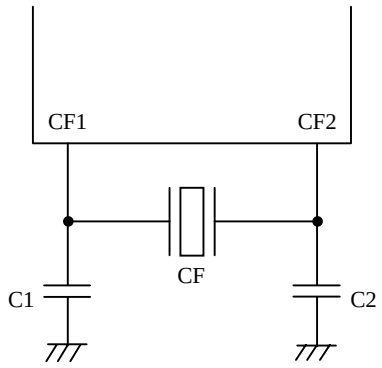


Figure 1 Ceramic oscillation circuit

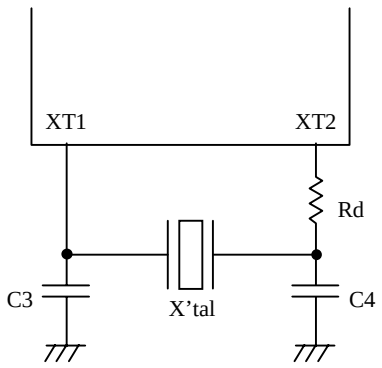


Figure 2 Crystal oscillation circuit

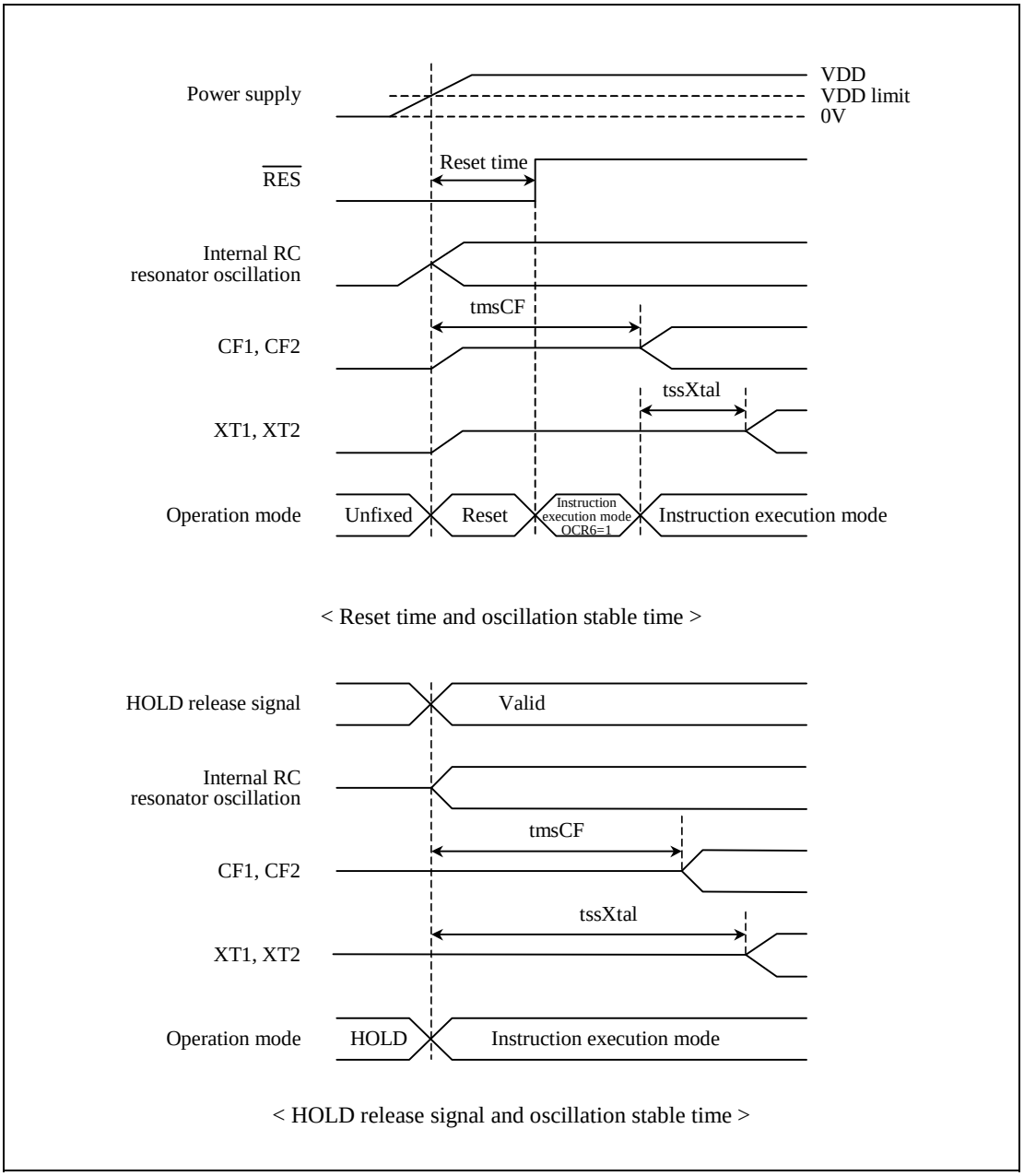
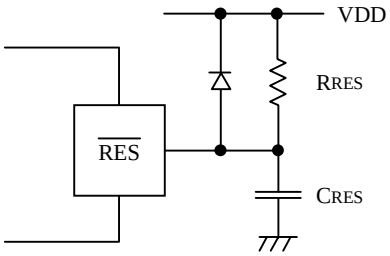
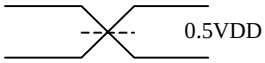


Figure 3 Oscillation stable time

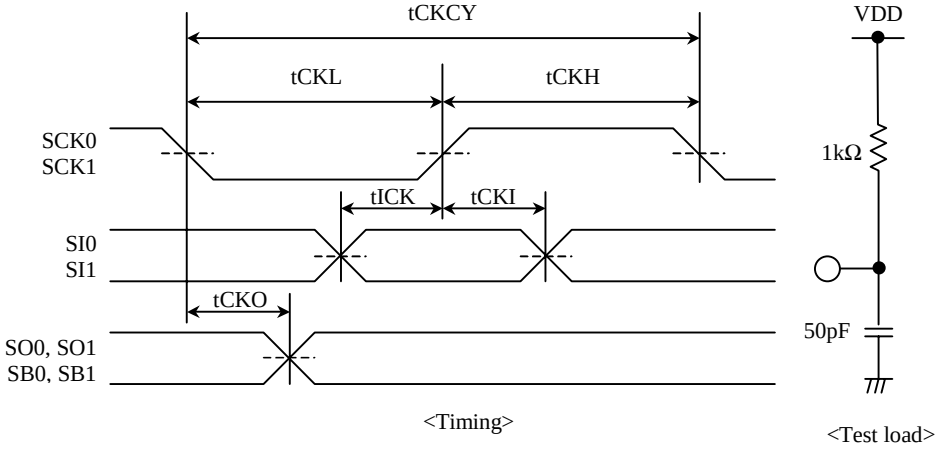


(Note) Fix the value of CRES, RRES that is sure to reset until 200μs, after Power supply has been over inferior limit of supply voltage.

Figure 4 Reset circuit



<AC timing point>



<Timing> <Test load>

Figure 5 Serial input / output test condition

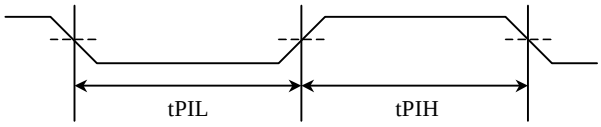


Figure 6 Pulse input timing condition